

REMARKS

Claims 9-13 and 15-18 are currently pending in the subject application. Claims 9, 17 and 18 have been amended herein for clarification purposes. Claims 10 and 15 have been cancelled herein. Favorable reconsideration in light of the amendments and remarks which follow is respectfully requested.

The Amendments

The claims have been amended to more particularly indicate novel aspects of applicants' invention. Such amendments are supported by the specification. In particular, the specification recites that "[t]ransistors other than ESD protection transistors ... may not be masked during [heavy doping of source and drain regions for the electrostatic discharge protection transistor]." (See pg. 9, ln. 22-23). As a result, claims 9, 17 and 18 (and claims 11-13 and 16 which depend therefrom) are believed allowable

The Obviousness Rejections

Claims 9 and 10 have been rejected under 35 U.S.C. §103(a) over Higashitani et al. (US 6,448,593 B1) in view of Huang (US 5,378,649). Claims 11 and 16 have been rejected under 35 U.S.C. §103(a) over Higashitani et al. in view of Huang and further in view of Diaz et al. ("Building-In ESD/EOS Reliability for Sub-Half Micron CMOS Processes," IEEE Trans. On Electron Devices, Vol. 43, No. 6, (1996) pp. 991-999). Claims 12 and 13 have been rejected under 35 U.S.C. §103(a) over Higashitani et al. in view of Huang and further in view of Reisinger (US 6,137,718). Claim 15 has been rejected under 35 U.S.C. §103(a) over Higashitani et al. in view of Huang and further in view of Shiue et al. (US 5,953,601). Claims 17 and 18 have been rejected under 35 U.S.C. §103(a) over Higashitani et al. in view of Huang and further in view of Diaz et al.

To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness, which requires that the prior art reference (or

references when combined) must teach or suggest all the claim limitations. See MPEP §706.02(j). Hagashitani et al. and Huang, alone and/or in combination, fail to teach or suggest all of the claim limitations. Additionally, Diaz et al., Reisinger and Shiue et al. fail to make up for the deficiencies of Hagashitani et al and Huang.

In particular, Hagashitani et al. and Huang, alone and/or in combination, fail to teach or suggest heavily doping source and drain regions for the electrostatic discharge protection transistors with the spacers in place and without masking the other transistors as recited in amended independent claim 9 (and similarly independent claims 17 and 18). Hagashitanti et al. discloses that after the LDD spacers are formed, a N+ implant mask is performed in step 74 followed by a N+ implant in step 76 to form N+ source and drain regions. (See col. 3, ln. 16-19). Thus, Hagashitanti et al. discloses utilizing a mask for heavy doping, which teaches away from heavily doping without masking as in applicants' claimed invention. Additionally, Huang merely relates to forming metal lines with smaller line pitches than is possible using conventional photolithographic single coating processes. (See abstract). Therefore, Hagashitani et al. and Huang fail to teach or suggest all of the claim limitations of applicants' claimed invention.

Moreover, Diaz et al., Reisinger and Shiue et al. fail to make up for the deficiencies of Hagashitani et al. and Huang. Diaz et al. merely discloses utilizing nDDD ESD implants for building in ESD/EOS reliability through nMOSFET drain design. (See pg. 1, Abstract). Reisinger merely relates to employing a dielectric triple layer having two silicon oxide layers separated by a silicon nitride layer to increase storage density in a memory cell. (See Abstract). Shiue et al. discloses forming a photoresist layer and patterning the ESD device to mask the internal FET devices from the damaging effects of implant ions. (See col. 5, ln. 17-23). Thus, Diaz et al., Reisinger and Shiue et al. do not teach or suggest heavily doping source and drain regions for the electrostatic discharge protection transistors with the spacers in place and without masking the other transistors as recited in applicants' claims.

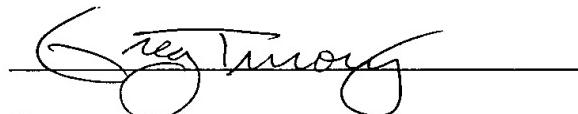
Applicants' invention provides benefits over prior art methods since the masking step prior to heavy doping is eliminated. Thus, applicants' claimed methods reduce costs associated with the prior art since the masking step is not performed. Accordingly, withdrawal of these rejections and allowance of claims 9, 17, and 18 (and claims 11-13 and 16 which depend therefrom) is respectfully requested.

Should the Examiner believe that a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact Applicants' undersigned attorney at the telephone number listed below.

In the event any fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to our Deposit Account No. 50-1063.

Respectfully submitted,

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